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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,349	11/25/2003	Hiromichi Watanabe	51580/DBP/A400	8245

23363 7590 10/04/2005

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EXAMINER	
SEMENENKO, YURIY	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,349	WATANABE ET AL.	
	Examiner	Art Unit	
	Yuriy Semenenko	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 May 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 2-10 are objected to because of the following informalities:
Claims 2-10, "A substrate" should be changed to -- the substrate-- for proper antecedence basis. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to

which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3.1. Claims 1-3 are rejected under 35U.S.C. 103(a) as being obvious over Admitted by Applicant (Prior Art, hereinafter "APA") in view of Daanen et al. (Patent # 6307749 hereafter "Daanen") .

3.1.1. Regarding claim 1: APA discloses in Fig.3 a substrate 1 for circuit wiring, in which an electronic component 4 is mounted by soldering 5 to a wiring pattern 3 formed on an insulated layer 2 deposited over a metallic substrate 1 (page 7, [0020]),

except, APA doesn't teach a mounting portion of said electronic component is resin-molded with a resin material, having a coefficient of linear thermal expansion smaller than the coefficient of linear thermal expansion of said insulated layer.

Daanen teaches in Fig. 3 a mounting portion of said electronic component 16 is resin-molded with a resin material 22 having a coefficient of linear thermal expansion 12-17ppm/^{0}C smaller than the coefficient of linear thermal expansion of said insulated layer (FR-4, column4, lines 45-47) (FR-4 has CTE = 25-30 ppm/^{0}C). Therefore, at time the invention was made, it was well know how to make a mounting portion of said electronic component is resin-molded with a resin material having a coefficient of linear thermal expansion smaller than the coefficient of linear thermal expansion of said insulated layer.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made for APA to include in his invention a mounting portion of said electronic

component is resin-molded with a resin material having a coefficient of linear thermal expansion smaller than the coefficient of linear thermal expansion of said insulated layer.

Benefit of doing so is to decrease stress in this over molded device.

3.1.2. Regarding claim 2: And further, APA, as modified, discloses in Fig.3 a substrate 1 for circuit wiring having all of the claimed features as discussed above with respect claim 1, wherein said insulated layer 2 is formed from a resin material containing an inorganic filler for increasing heat dissipation and an elastic filler for reducing an elastic modulus (silica-based filler, page 4, [0009] and [0011]).

3.1.3. Regarding claim 3: And further, APA, as modified, discloses in Fig.3 a substrate 1 for circuit wiring having all of the claimed features as discussed above with respect claims 1 or 2,

except, APA doesn't teach the coefficient of linear thermal expansion of said resin material for said resin-molding is adjusted by adding an inorganic filler.

Daanen teaches in Fig. 3 the coefficient of linear thermal expansion of said resin material for said resin-molding is adjusted by adding an inorganic filler (column 4, lines 57-65). At time the invention was made, it was well know how to adjuste the coefficient of linear thermal expansion of said resin material for said resin-molding by adding an inorganic filler. Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made for APA to include in his invention the coefficient of linear thermal expansion of said resin material for said resin-molding is adjusted by adding an inorganic filler.

Benefit of doing so to decrease stress in this over molded device.

3.2. Claims 4-10 are rejected under 35U.S.C. 103(a) as being obvious over APA in view of Daanen and in view of Shimizu et al. (Patent # 6201696 hereafter "Shimizu").

3.2.1. Regarding claims 4, 5, 8 and 9: And further, APA, as modified, discloses in Fig. 3 a substrate for circuit wiring having all of the claimed features as discussed above with respect claim 3 (7),

except, APA doesn't teach said inorganic filler has electrical insulation properties and high thermal conductivity and wherein said inorganic filler comprises one or more materials selected from the group consisting of silicon oxide, aluminum oxide, aluminum nitride, silicon nitride, and boron nitride.

Shimizu teaches said inorganic filler has electrical insulation properties and high thermal conductivity and wherein said inorganic filler comprises one or more materials selected from the group consisting of silicon oxide, aluminum oxide, aluminum nitride, silicon nitride, and boron nitride (column 14, lines 53-67 and column 15, lines 1-6). Therefore, at time the invention was made, it was well know said inorganic filler has electrical insulation properties and high thermal conductivity and wherein said inorganic filler comprises one or more materials selected from the group consisting of silicon oxide, aluminum oxide, aluminum nitride, silicon nitride, and boron nitride.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made for APA to include in his invention said inorganic filler has electrical insulation properties and high thermal conductivity and wherein said inorganic filler comprises one or more materials selected from the group consisting of silicon oxide, aluminum oxide, aluminum nitride, silicon nitride, and boron nitride.

Benefit of doing so to improve robust of the device and give a possibility of using chipper substrate.

3.2.2. Regarding claims 6 and 10: And further, APA, as modified, discloses in Fig. 3 a substrate 1 for circuit wiring having all of the claimed features as discussed above with respect claim 5, herein said metallic substrate is aluminum based (page 2, [0005]).

3.2.3. Regarding claim 7: APA, as modified, discloses in Fig. 3 a substrate 1 for circuit wiring having all of the claimed features as discussed above with respect claim 1 or 2, wherein the mounting portion of said electronic component is molded with said resin material with said insulated layer and said metallic substrate in integral fashion (see Daanen , Fig. 3).

Relevant Art

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

4.1. Regarding Brandenburg et al. (Patent # 6779260 hereafter "Brandenburg") Brandenburg discloses in Fig. 3 a substrate 24 for circuit wiring, in which an electronic component 30 is mounted by soldering 34 to a wiring pattern formed on an insulated layer deposited over a metallic substrate, wherein a mounting portion of said electronic component is resin-molded with a resin material 110 having a coefficient of linear thermal expansion 6-8 ppm/^{0}C smaller than the coefficient of linear thermal expansion of said insulated layer (column 6, lines 15-65).

5.1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

5.2. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571)- 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

5.3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YS

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